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Design and Implementation of Vending Machine Controller using VHDL

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ABSTRACT
A vending machine is an example of automated machine which provides us items like snacks, chocolates, beverages, and movie tickets to customers after payment is done. It can be made online or cash any way. In this busy life schedule it is time saving. This paper describes design and implementation of vending machine using Finite State Machine (FSM) machine.The design is simulated in VHDL and implemented on Basys 3 FPGA board.

Keyword: FSM, VHDL, Vending Machine, Basys 3board.

I. INTRODUCTION

A vending machine are self-operated machine which are found in public areas such as schools, offices, shopping malls, and airports, providing convenient access to goods without the need for human assistance.The first modern vending machines were produced in England in the early 1880s and dispensed postcards. The earliest known instance of a vending machine is

In the work of Hero of Alexandria, an engineer, and maths professor in first-century Roman Egypt [1]. Nowadays, these can be found everywhere like at railway stations selling train tickets, in schools and offices vending drinks and snacks, in banks as ATM machine and provides even diamonds and platinum jewellers to customers. In this machine we can easily increase and decrease the number of products.

Operation - Vending Machine
The process for operation of vending machine proposed in this paper is described below.
1. Customers insert money in vending machine.
2. Vending machine check and then tells controller that how much money is inserted.
3. Customers select the items.
4. Controller accept the command and give the product to Customers.

Finite State Machine
FSM stands for Finite state machine used by programmers, engineers and other professionals to describe a mathematical model for any system that has a limited number of conditional states of being.There are two types of FSM 1. Mealy and 2. Moore [2].

1-Mealy Machine:
Mealy machine is a machine whose output values are depends on both current state and the current inputs.The block diagram of Mealy machine is as shown in fig 1,

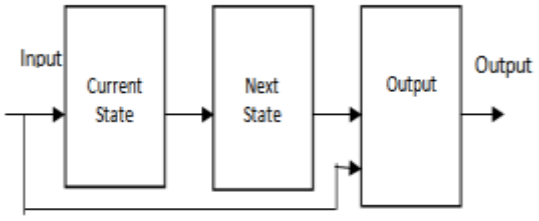

Fig.1: Mealy machine

1 - Moore Machine:
Moore machine states that a finite-state machine whose current output values are depends only on its current state.The block diagram of Moore machine is as shown in fig 2,

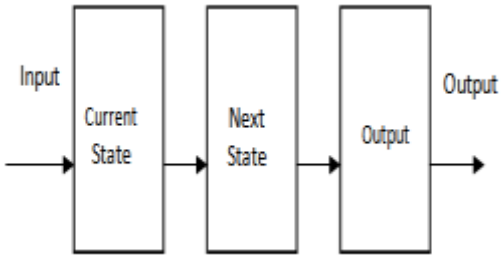

Fig. 2: Moore Machine

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2 Operation of Vending Machine

This section describes the operation of vending machine along with its state diagram. In our vending machine we have two products that is 'Product a' and 'Product b'. At first the quantity of the items required are selected. Then we can review that we have selected is write or wrong if wrong we can select is once again. If write then it we can insert coin in it. This machine is made only for insertion of up to 10 Rs. We can't insert more than that this is drawback of our machine.

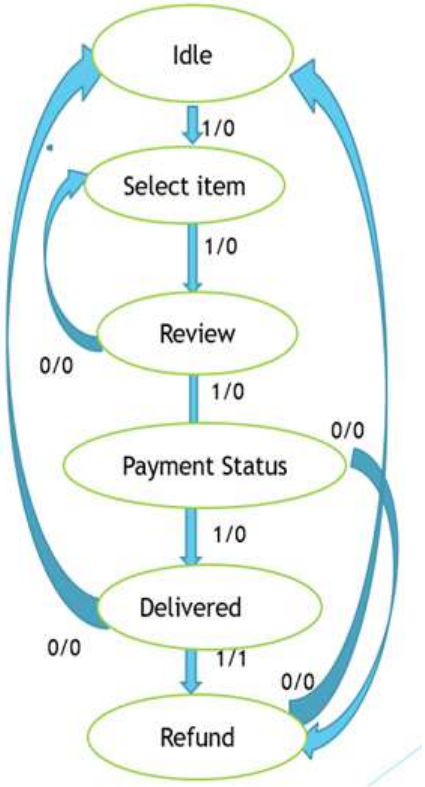
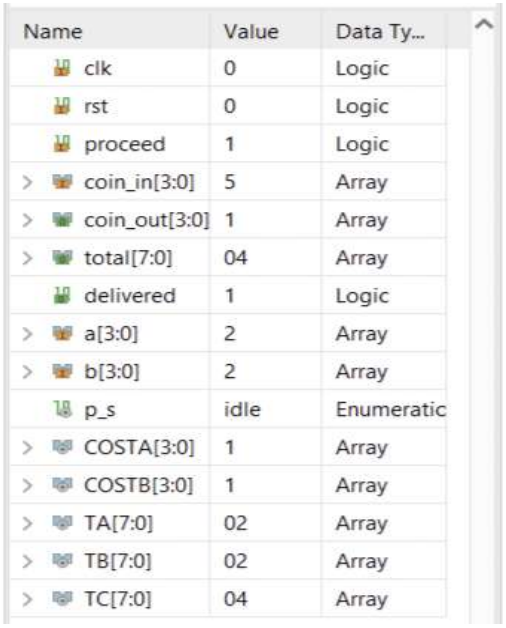


Fig.3: State diagram of Vending Machine

If our inserted money is sufficient then it will give us the selected product. If not it will not give the selected products. Then it willidle state again. If we have inserted more money than the total, then it will give us coin in - total money out.

II. DESIGN

In this section we have defined how we have designed the vending machine clk is for giving the clock plus o or 1 in program. rst is for taking the vending machine back to idle state. proceed is for processing data. Coin_in- inserting money in vending machine.Input output are given in diagram below



Name	Value	Data Ty...
clk	0	Logic
rst	0	Logic
proceed	1	Logic
coin_in[3:0]	5	Array
coin_out[3:0]	1	Array
total[7:0]	04	Array
delivered	1	Logic
a[3:0]	2	Array
b[3:0]	2	Array
p_s	idle	Enumeratic
COSTA[3:0]	1	Array
COSTB[3:0]	1	Array
TA[7:0]	02	Array
TB[7:0]	02	Array
TC[7:0]	04	Array

Fig:4input output

coin_out for taking the money that is more than total which is delivered by the machine. Total is the total amount of the products. Product is delivered to the customer a,b are the quantity of the products TA and TB. .a is quantity of TA that is a item and b is quantity of TB.

VHDL Process:

Process(clk,rst,p_s,coinin)
Stdlogicvector(3downto0);
• begin
•if (rst='1')then
•p_s <= idle; elsif(clk′ eventandclk =′ 1 ′)then
•case p_siswhenidle =>
•p_s <=selectitem;whenselectitem =>
• TC¡=(TA + TB);
•p_s <=review;whenreview => 3
•if(proceed='1')then
•p_s <= paymentstatus; elsif(proceed =′ 0 ′)then
•p_s <= selectitem; endif;
•whenpaymentstatus => if(T C <= coinin) then • delivered ¡= '1';
•p_s <= refund; elsif(T C > coinin)then
• delivered¡='0';
•coinout <= coinin; p_s <= paymentstatus;
• end if;
•when refund
•coinout <= coinin − TC(3downto0); p_s <= idle

In first process if rst is 1 then the present state goes to idle state.In next process it goes to select items state we can select items like TA and TB.Next we can insert how many means quantity of the items can be inserted.[4]

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Next process is review state in that state we can see or we can check that the number or quantity that we have inserted is write or wrong
If proceed is 1 then it will go to payment status or if proceed is 0 then it will go to again select items state.
If coin_ in is more than total or equal to total then the item is delivered otherwise wise not delivered. It goes again to payment status.
If coin_in is more than the total we get coin_in - total this Amount of money out. In last when all this process is done then state goes to idle state again.

4 Basys 3 Board

Diligent Inc. created the development board known as the Basys 3. It was made specifically for using FPGAs (Field-Programmable Gate Arrays) to teach and learn digital design. Here are some details regarding the Basys 3:FPGA: A Xilinx Artix-7 FPGA is present on the Basys 3 board. A well-liked FPGA family is the Artix-7, which is renowned for both its excellent performance and low power requirements [3]

I/O Interfaces: The board offers a range of input/output interfaces, including 4 Pmod connectors, 16 Pmod switches, 16 Pmod LEDs, 5 buttons, 8 seven-segment displays, and numerous more I/O ports. Users can interact with the board and implement various digital designs using these interfaces. A 100 MHz clock oscillator built into the Basys 3 offers a reliable clock source for your designs. It also provides a clock.
Basys 3 Board is shown in fig below,
Basys 3 kit

Fig 5: basys 3 board

III. SIMULATION RESULTS

There are 12 mux in the gate diagram. There are 2 MP ICs in the ckt that we have taken in code. In this ckt at left most side there are inputs which are rst, proceed, coin_in, a, b. And at right most side there are outputs that are coin_out, delivered, total. RTL design is shown in Fig.

The state diagram is implemented on vivado software and we get the output as this simulation. Waveform for the two products TA and TB is simulated for quantity a and b. Let's see an example for this- First we insert 5 Rs. We have selected a = 2 and b = 2. So the total cost become 4 rupees we inserted 5 rupees so the products will be delivered and the coin out will be 1 rupee.

If the coin in is less than total then the product will not be delivered. If coin in is greater than total than product will delivered and refund is given

Timing analysis
It is used for knowing how much time that process is using for implementing it,

Figures given below shows the timing analysis of code,

Setup

Worst Negative Slack(WNS)	5.387 ns
Total Negative Slack (TNS)	0.000 ns
Number of failing Endpoints	0
Total Number of Endpoints	30

Hold

Worst Hold Slack (WHS)	0.179 ns
Total Hold Slack (THS)	0.000 ns
Number of failing Endpoints	0
Total Number of Endpoints	30

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Pulse Width

Worst Pulse Width Slack (WPWS)	4.500 ns
Total Pulse Width Negative Slack (TPWS)	0.000 ns
Number of failing Endpoints	0
Total Number of Endpoints	21

Utilization design

Fig given below shows the graph of utilization of code. In which IO is used most that is 26% and other LUT, FF, BLFG are used 1,1and 3% respectively.

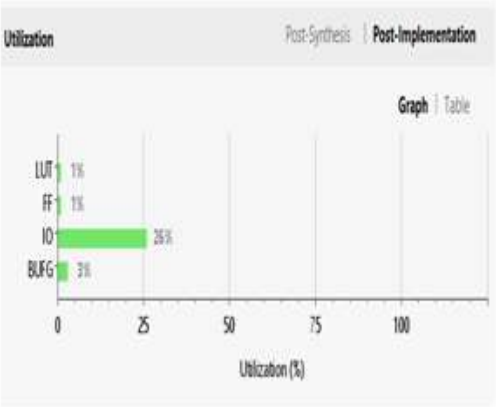

Fig: 6Device utilization reportUtilization

Power

Total On Chip Power	0.076 W
Design Power Budget	Not Specified
Power Budget Margin	N/A
Junction Temperature	25.4 c
Thermal Margin	59.6c(11.9W)
Effective 0JA	5.0c/W
Power supplied to off-chip devices	0W
Confidence level	Low

In the above diagram the power usage table and graph is given that tells us about how much power is used all the components like here on chip power is used that is 0.076 W.

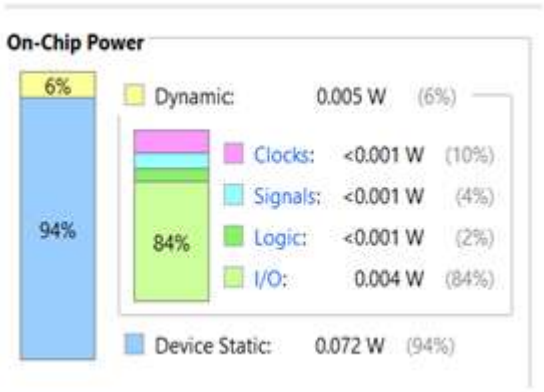

Fig 7

IV. CONCLUSION

This paper has presented design and implementation of vending machine using FSM which is implemented using Vivado using VHDL. It is implemented on the basys 3 board. The RTL design, device utilization summary, power and timing reports have been presented. The work can be extended further to implement it in real time with add on sensors.

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In the below diagram our simulation is shown,

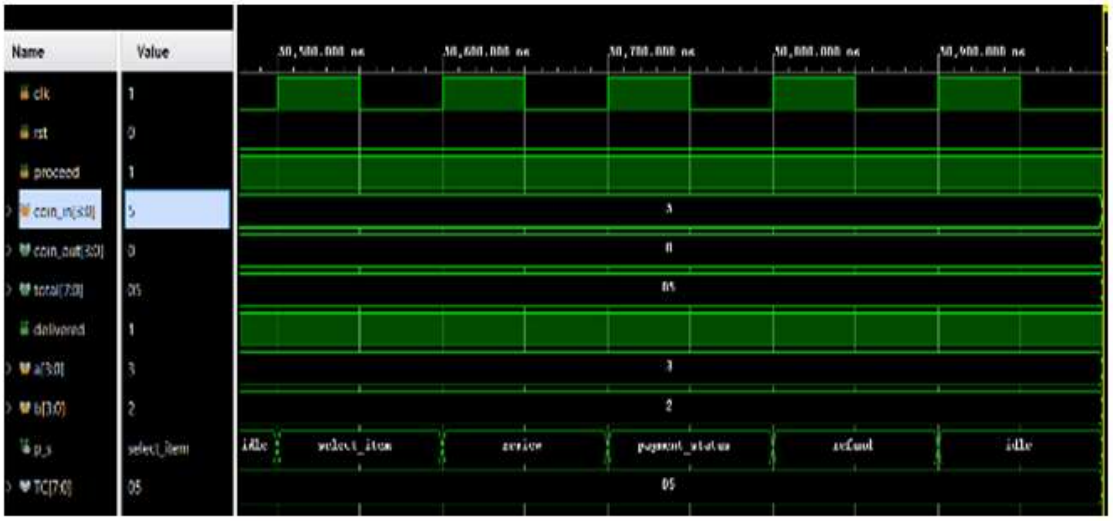

Fig 8: simulation

In the below diagram RTL design is shown,

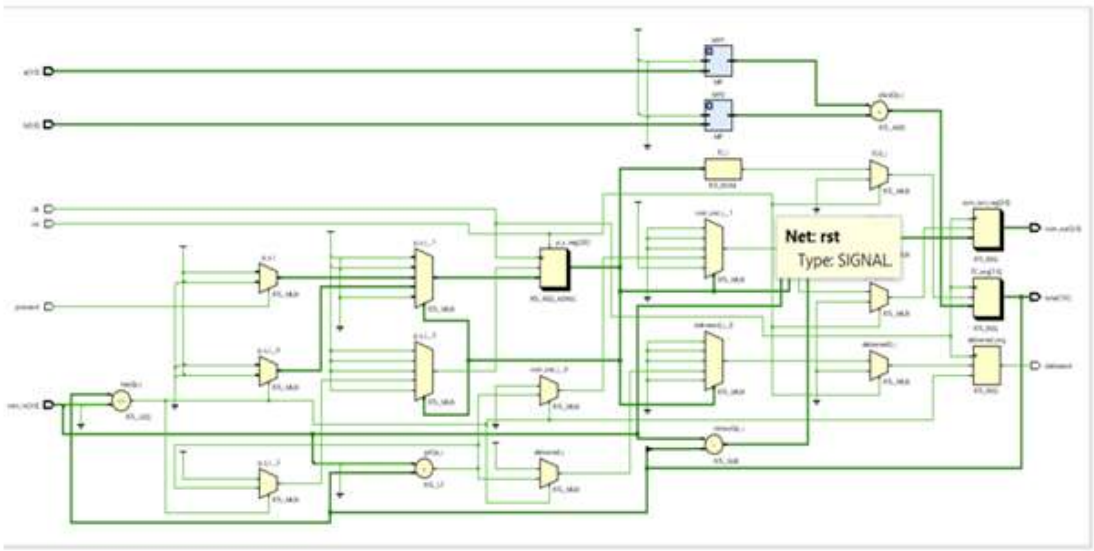

Fig 9: RTL design